

The diagram illustrates a system architecture with the following components and connections:

- Processors (2):** Four identical blocks labeled "Wmt/Foster" are connected to the FSB via a bus.
- FSB (4):** Front Side Bus, represented by a horizontal line with an upward-pointing arrow.
- MCH (6):** Memory Controller Hub, a large central block containing "Re-Direction Logic".
- Memory Channels:**
  - 8 bit HL\_A (12):** Connected to the MCH and the ICH2.
  - 16 bit HL\_B (16):** Connected to the MCH and the P64H.
  - 16 bit HL\_C (8):** Connected to the MCH and the P64H.
  - AGP/PCI (or 16 bit HL\_D,E) (10):** Connected to the MCH and the AGP Device.
- ICH2 (12):** I/O Controller Hub 2, containing an "IOx APIC".
- P64H (16):** P64H (PCI-to-AGP Bridge), containing an "IOx APIC".
- AGP Device (or 2 P64H) (20):** Connected to the AGP/PCI channel.
- PCI Devices:**
  - PCI 32/33 (26):** Connected to the ICH2.
  - PCI 64/66 (22):** Connected to the P64H.
  - PCI Device (24):** Connected to the PCI 64/66 bus.

FIG. 1

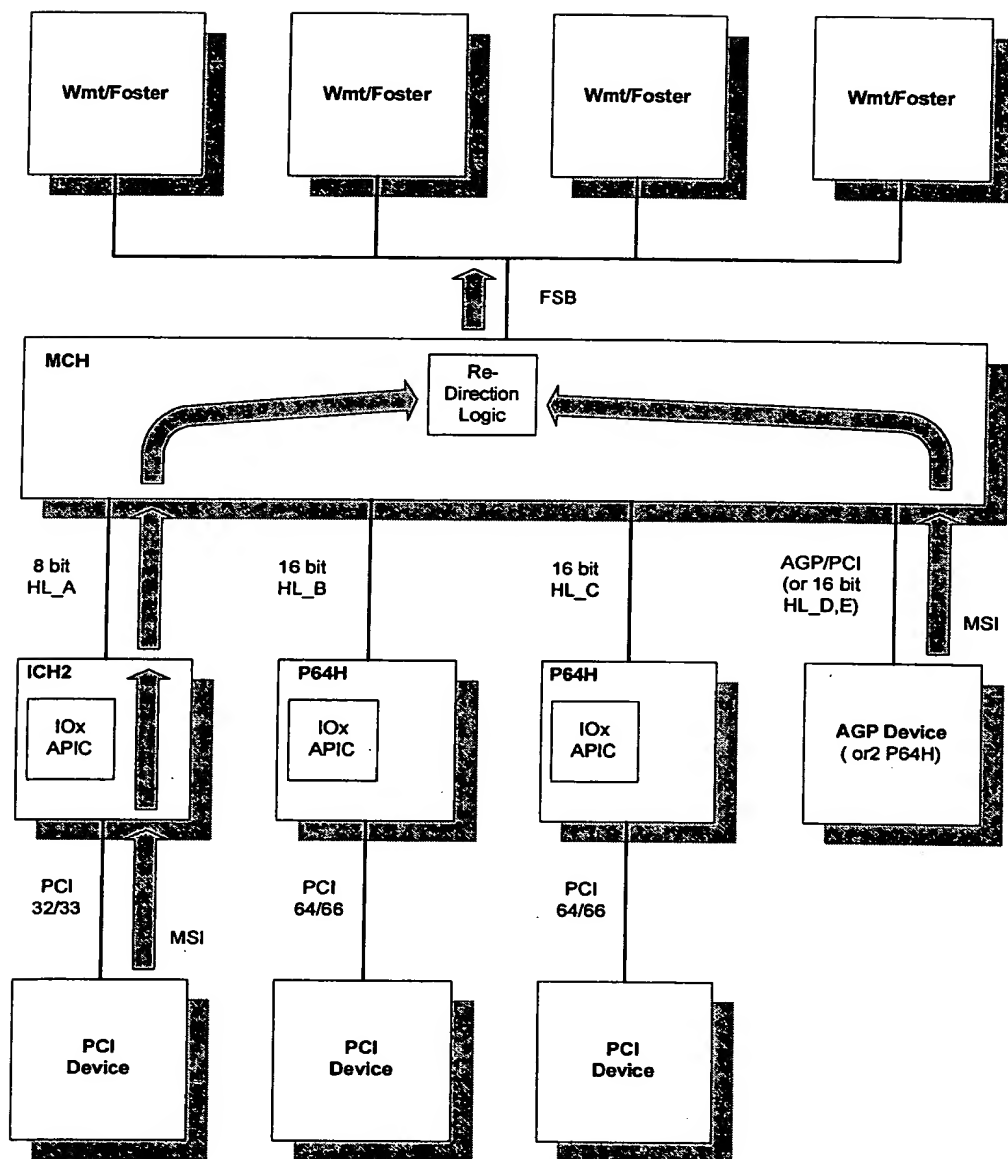


FIG. 2

The diagram illustrates the Intel® Pentium® Pro system architecture. At the top, four **Wm/Foster** modules are connected to a central **FSB** (Front Side Bus). Below the FSB is the **MCH** (Memory Controller Hub), which contains **Re-Direction Logic**. The MCH is connected to four main components: **ICH2** (I/O Controller Hub 2) on the left, **P64H** (P64 Controller Hub) in the middle, **P64H** on the right, and an **AGP Device (or 2 P64H)** on the far right. The ICH2 is connected to an **IOx APIC** and a **PCI Device** via **PCI 32/33** and **MSI** lines. The P64H units are connected to **IOx APIC**s and **PCI Devices** via **PCI 64/66** lines. The AGP Device is connected to the system via **AGP/PCI (or 16 bit HL\_D,E)** lines. The diagram also shows **8 bit HL\_A**, **16 bit HL\_B**, and **16 bit HL\_C** lines connecting the MCH to the ICH2 and P64H units.

FIG. 3

Figure 1 consists of 15 small, vertically stacked diagrams illustrating the stages of larval development. Each diagram is labeled with a number from 1 to 15. The diagrams show a progression from a small, rounded egg-like form at the top to a more elongated, segmented larva in the middle, and finally to a pupa at the bottom. The segments of the larva and pupa are clearly defined, and the overall shape becomes more complex as the stage number increases.

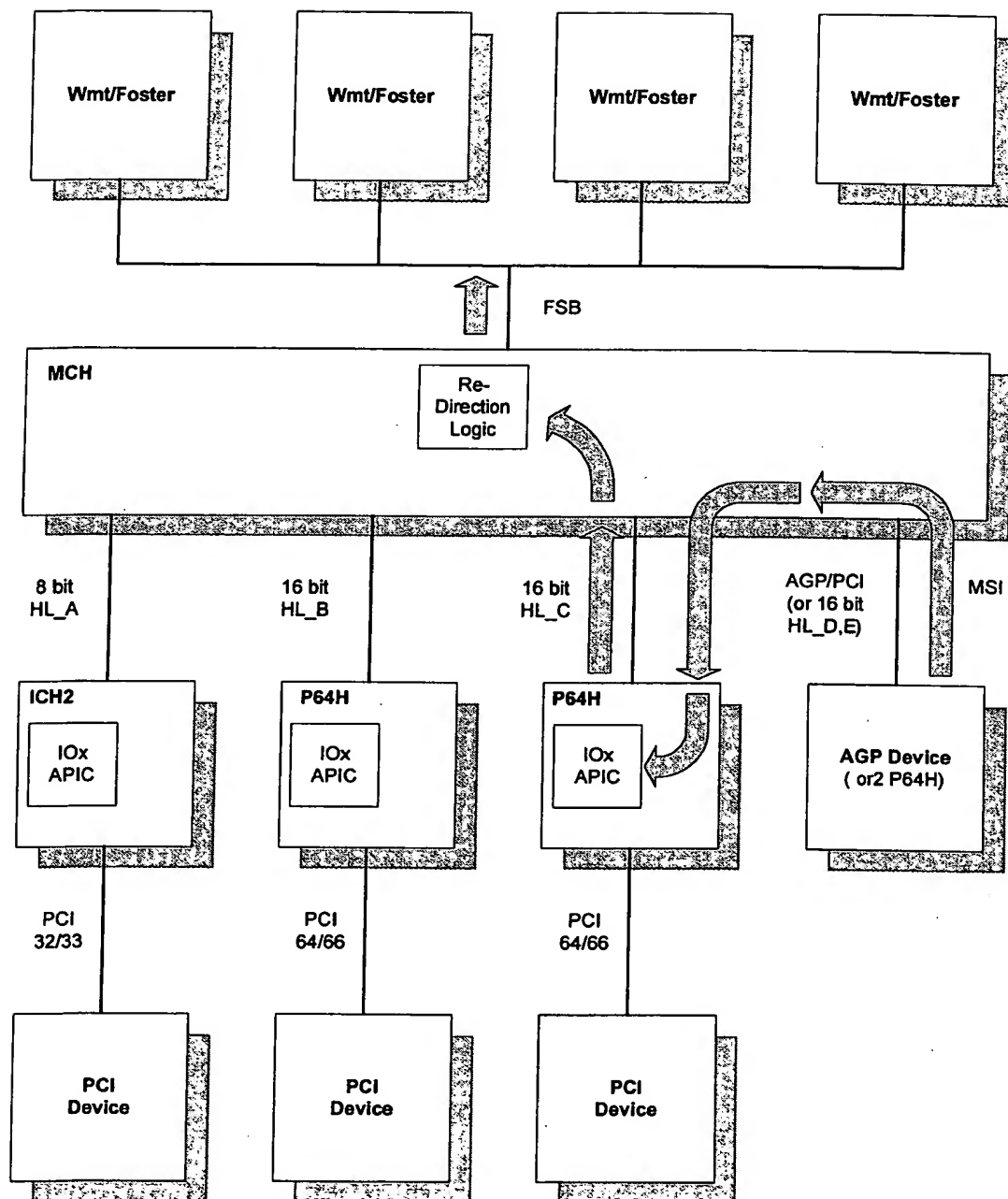


FIG. 4

The diagram illustrates the hardware components and their interconnections. At the top, four identical blocks are labeled "Wmt/Foster". Each block is connected to a common horizontal bus. Below this bus, on the left, is a large block labeled "MCH". A vertical line connects the bus to the MCH block. To the right of the MCH block, there is a smaller block labeled "Re-Direction Logic". A curved arrow points from the "Re-Direction Logic" block to the bus. Further to the right, another curved arrow points from the bus to a block labeled "FSB". To the far right, a block labeled "IPI" is partially visible, with a curved arrow pointing from it to the "FSB" block. The "FSB" block is connected to the "Re-Direction Logic" block by a curved arrow pointing from the "FSB" block to the "Re-Direction Logic" block.

FIG. 6